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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/587,662	07/26/2006	Gerhard Kottschlag	10191/4355	8299

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EXAMINER	
POOS, JOHN W	
ART UNIT	PAPER NUMBER
2816	
MAIL DATE	DELIVERY MODE
02/02/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/587,662	KOTTSCHLAG, GERHARD	
	Examiner	Art Unit	
	JOHN W. POOS	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9,12,14 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14 and 15* is/are allowed.

6)☒ Claim(s) *9 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 9, 12, and 14-15 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 9 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Heidemann et al. (US 5,302,922).

In regard to Claim 9 (as taught in Figure 6):

The varactor diode alternative circuit as recited in claim 12, wherein the at least one of the resistor network and the inductor network (L1-L3 and Rb1-Rb3, and the three Rs's) is arranged so that anodes of the varactor diodes, with respect to the control voltage supplied to the circuit, are connected to a first electrical potential (Ub2), and cathodes of the varactor diodes, with respect to the control voltage, are connected to a second electrical potential (Ua2) that is higher, by the control voltage, compared to the first electrical potential (Figure 1 shows that Ua is larger than Ub).

In regard to Claim 12 (as taught in Figure 6):

A varactor diode alternative circuit, comprising:

at least three varactor diodes that are in each case connected in series alternatingly opposite to one another; and (Cb2, C8, Cg, and Ca2)

at least one of a resistor network and an inductor network, the at least one of the resistor network and the inductor network coupled to the at least three varactor diodes; (L1-L3 and Rb1-Rb3, and the three Rs's)

wherein:

at each of the varactor diodes, a control voltage supplied to the circuit for adjusting capacitance is applied at least approximately at full extent (Ub2 and Us2)), and an alternating voltage that is applied at the series connection of the varactor diodes, which is at a higher frequency compared to the control voltage, is distributed at least approximately uniformly to the varactor diodes (Column 8: lines 58-61);

the at least three varactor diodes include one of an even number of varactor diodes and an even number of parallel connections of varactor diodes; (Cb2, C8, Cg, and Ca2)

at each node of the series connection, respectively either anodes of the varactor diodes or cathodes of the varactor diodes are connected to one another; (Cb1, C8, Cg, and Ca1 in parallel with Cb2, C8, Cg, and Ca2 in parallel with Cb3, C8, Cg, and Ca3)

nodes of the cathodes lying between outside terminals are connected via at least one of resistors and inductors (Rb2 and Rs) to the cathodes of the varactor diodes whose cathodes form a first outside terminal (Ub2) and a second outside terminal (Us2) of the alternative circuit; and

nodes of the anodes lying between the outside terminals being connected to one of resistors and inductors (Ra2 and L2) whose second terminals form a control voltage terminal (Ck terminal) for supplying the control voltage to set the capacitance.

Allowable Subject Matter

4. Claims 14 and 15 are allowed.

5. The following is a statement of reasons for the indication of allowable subject matter:

In regard to Claim 14:

None of the prior art of record is seen to disclose or suggest the limitation of claim 14 that an oscillator circuit having a tunable oscillating frequency and a varactor diode alternative circuit configured to tune the oscillating frequency by adjusting a capacitance of the alternative circuit in response to a control voltage.

For example, the closest reference found, Heidemann (US 5,302,922), teaches at least three varactor diodes that are in each case connected in series alternatingly opposite to one another; and at least one of a resistor network and an inductor network, the at least one of the resistor network and the inductor network coupled to the at least three varactor diodes; wherein: at each of the varactor diodes, the control voltage is applied at least approximately at full extent, and an alternating voltage that is applied at the series connection of the varactor diodes, which is at a higher frequency compared to the control voltage, is distributed at least approximately uniformly to the varactor diodes; the at least three varactor diodes include one of an even number of varactor diodes and an even number of parallel connections of varactor diodes; at each node of the series connection, respectively either anodes of the varactor diodes or cathodes of the varactor diodes are connected to one another; nodes of the cathodes lying between outside terminals are connected via at least one of resistors and inductors to the cathodes of the varactor diodes whose cathodes form a first outside terminal and a second outside terminal of the alternative circuit; and nodes of the anodes lying between the outside terminals being connected

to one of resistors and inductors whose second terminals form a control voltage terminal for supplying the control voltage to set the capacitance, but does not teach an oscillator circuit having a tunable oscillating frequency and a varactor diode alternative circuit configured to tune the oscillating frequency by adjusting a capacitance of the alternative circuit in response to a control voltage.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN W. POOS whose telephone number is (571)270-5077. The examiner can normally be reached on M-F (alternating Fridays off), 8:00 a.m - 4:00 p.m E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kenneth B Wells/
Primary Examiner, Art Unit 2816

/J. W. P./
Examiner, Art Unit 2816